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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/647,607	08/25/2003	S. Brandon Keller	100111259-1	2819

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EXAMINER	
DOAN, NGHIA M	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 05/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/647,607	KELLER ET AL.	
	Examiner	Art Unit	
	Nghia M. Doan	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 March 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01/17/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Responsive to communication application 10/647,607 filed on 08/25/2003 and Applicant Amended filed on 03/20/2006, claims 1-20 are pending.

Claim 4 has been amended.

2. The new drawing filed on 03/20/2006 is accepted.

3. The specification amended is accepted.

4. The Claim Objection has been obviated.

5. Applicant's arguments filed 03/20/2006 have been fully considered but they are not persuasive. Therefore, the claim rejection is maintained.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Buchanan (US PG Pub. 2003/0005394 A1).

8. **With respect to claims 1 and 19-20**, Buchanan discloses a method (abstract), system (fig. 1, see ¶23-¶27), and computer product (abstract) for identifying data sources associated with a circuit design (abstract), comprising:

(means for/ instruction for) retrieving data source information including identification of a data source used to generate data for an entity in a design portion of

interest in the circuit design (*page 2, ¶18– retrieve and output an identifier associated with the cell from the database, where maintains a plurality of cell characteristics – ; page 5, ¶50, -- retrieved comparable data from compilers and other source. More particularly, when recording characteristics from library-derived cells may receive file or reports generated from remote library design entities. The file may contain compatible identifiers--; and page 5, ¶51, -- retrieve identifiers and related data from other database containing library source--*);

(means for/ instruction for) formatting the data source information as a bit vector (*a stream of binary bits*) associated with the entity (*page 3, ¶33, -- the file to have specific manufacturing syntax and formats may include CIF or GDS, which is conventionally comprise a stream of binary bits that encode a sequence of records, which may related to descriptions of logical unit or cell, etc* --), wherein each of a plurality of bits in the bit vector comprises indicia applicable to the entity (*page 3, ¶35, program code may assess the size, placement and /or sequence of registered bits to determine the nature of the record. Tags and other indicators programmed into the manufacture code may further provide a means for distinguishing cell records from other header data*--); and

(means for/ instruction for) processing the bit vector to generate formatted output (*page 3,* ¶18, -- *output an identifiers associated with the cell from database--; page 5,* ¶51, -- *generating a library report as well as the extraction of identifying information and characteristics and related data from other database containing library resources -- page 5, ¶50, -- reports generated form remote library design entities --; and page 6,* ¶70,

the library reports may document cell characteristic that program code may process to arrive at an identifiers --).

9. **With respect to claim 2**, Buchanan discloses the method of claim 1, wherein the entity is at least one design element in the design portion of interest (*page 5, ¶50 and ¶54, -- the compiler signature file into the design database and compiler produces and place an appropriate identifier into a portion of the IC design file* --).

10. **With respect to claim 3**, Buchanan discloses the method of claim 1, wherein the entity is a group of design elements in the design portion of interest (*page 5, ¶50 and ¶54 (same as claim 2) and page 5, ¶47, -- an identifier may correspond to cell on a one-to-one basis, as well as to group of cells sharing a common characteristic or collection of characteristic* --).

11. **With respect to claim 4**, Buchanan discloses the method of claim 1, wherein the entity is an HLSN *(cell name)(--inherent from libraries make cell available for automatic placement and routing with in a custom semiconductor layout – page1, ¶6))* in the design portion of interest (*page 5, ¶50 and ¶54 (same as claim 2) and page 4, ¶43 and ¶47*).

12. **With respect to claim 5**, Buchanan discloses the method of claim 1, wherein the entity is a net *(--inherent from libraries make cell available for automatic placement and routing with in a custom semiconductor layout – page1, ¶6)* in the design portion of interest (*page 5, ¶50 and ¶54 (same as claim 2) and page 4, ¶43 and ¶47*).

13. **With respect to claim 6**, Buchanan discloses the method of claim 1, wherein the indicia includes information that identifies at least one specific data source applicable to the entity (*page 3, ¶33, -- the file to have specific manufacturing syntax and formats*

may include CIF or GDS, which is conventionally comprise a stream of binary bits that encode a sequence of records, which may related to descriptions of logical unit or cell, etc --).

14. **With respect to claim 7**, Buchanan discloses the method of claim 1, wherein the step of retrieving further includes retrieving information that identifies a type of analysis performed by the CAD tool (*Graphic Design System [GDS] or Caltech Intermediate Format [CIF]), and wherein the indicia identifies a specific type of the analysis (--header records that may be peripheral to the present application, which is the data header is specified what type of CAD tool will be used to perform analysis --; page 3, ¶33-¶35 and page 5, ¶51 and ¶53).*

15. **With respect to claim 8**, Buchanan discloses the method of claim 1, wherein the step of retrieving includes retrieving data source information that identifies limits that were applied to numeric quantities in the analysis *(page 4, ¶40, characteristic may involve a unique, numeric value or signature, which uses a checksum algorithm, such as transmit 16 bits of a cell to an adder, or evaluate an entire cell string by dropping a least significant bit from the register, and then adding a next occurring bit to the accumulating value of the cell count. Moreover, checksum algorithm is useful in verifying the integrity of already identified cells--)* and wherein the indicia identifies the limits (*page 6, ¶66-¶68, -- a characteristic or set of characteristic unique to particular cell in the file and program code may evaluated and relied one or more characteristic (involved a numerical signature or checksum value to monitor cells or cells function within the file*).

16. **With respect to claim 9**, Buchanan discloses the method of claim 1, wherein the step of retrieving includes retrieving data source information that identifies errors that occurred while processing a design element, and wherein the indicia identifies the errors (*page 5, ¶55, -- a designer may type in or otherwise indicate the identifier that corresponds to the defective cell-- , page 5, ¶55, --program code compare the identifiers of the cells contained in the file with the designated identifier, a match to be detected, and the designer may substitute a suitable cell for the identified defective one* --).

17. **With respect to claim 10**, Buchanan discloses the method of claim 1, further comprising displaying the bit vector *(computer system, figure 2, and ¶23-¶27)*

18. **With respect to claim 11**, Buchanan discloses the method of claim 1, further comprising storing the bit vector in a file (*abstract, -- a database configured to store and recall the identifier and characteristic along with additional properties that pertain to the cell, see figures 1 and 2 and ¶23-¶27)*

19. **With respect to claim 12**, Buchanan discloses the method of claim 1, wherein the bit vector is overloaded such that a specific subset of a plurality of bits therein has a significance dependent on the specific subset and on usage context of the bit vector (*page 4, ¶40, -- evaluated an entire cell string by dropping a least significant bit, and then adding a next occurring bit to accumulating value of the cell count*--).

20. **With respect to claim 13**, Buchanan discloses the method of claim 1, wherein the indicia identifies a specific type of the analysis (*(--header records that may be peripheral to the present application, which is the data header is specified what type of CAD tool will be used to perform analysis --; page 3, ¶33-¶35 and page 5, ¶51 and ¶53).*

21. **With respect to claim 14**, Buchanan discloses the method of claim 1, wherein the indicia identifies limits that were applied to numeric quantities in the analysis *(page 4, ¶40, characteristic may involve a unique, numeric value or signature, which uses a checksum algorithm, such as transmit 16 bits of a cell to an adder, or evaluate an entire cell string by dropping a least significant bit from the register, and then adding a next occurring bit to the accumulating value of the cell count. Moreover, checksum algorithm is useful in verifying the integrity of already identified cells--)*.

22. **With respect to claim 15**, Buchanan discloses the method of claim 1, wherein the indicia identifies errors that occurred while processing a design element in the design portion of interest (*page 5, ¶55, -- a designer may type in or otherwise indicate the identifier that corresponds to the defective cell-- , page 5, ¶55, --program code compare the identifiers of the cells contained in the file with the designated identifier, a match to be detected, and the designer may substitute a suitable cell for the identified defective one –)*.

23. **With respect to claim 16**, Buchanan discloses a system (fig. 1, see ¶23-¶27) for identifying a data source used by a CAD tool in analysis of a circuit design, wherein a plurality of data sources are available to the CAD tool, comprising:

a processor coupled to a computer memory (fig. 1, see ¶23-¶27);

a plurality of data source indicators, stored in the computer memory (fig. 1, see ¶23-¶27), each of which comprises a plurality of bits for identifying the data sources associated with an entity in a design portion of interest in the circuit design (*page 2, ¶18– retrieve and output an identifier associated with the cell from the database, where maintains a plurality of cell characteristics – ; page 5, ¶50, -- retrieved comparable data*

from compilers and other source. More particularly, when recording characteristics from library-derived cells may receive file or reports generated from remote library design entities. The file may contain compatible identifiers--; and page 5, ¶51, -- retrieve identifiers and related data from other database containing library source--); and

a table (*fig. 4, ¶47, retrieve an identifier associated with the characteristic field from the column (table) of identifier fields*), stored in the computer memory (fig. 1, see ¶23-¶27), for formatting the data source indicators (*page 3,* ¶18, -- *output an identifiers associated with the cell from database--; page 5,* ¶51, -- *generating a library report as well as the extraction of identifying information and characteristics and related data from other database containing library resources -- page 5, ¶50, -- reports generated form remote library design entities --*; *and page 6,* ¶70, *the library reports may document cell characteristic that program code may process to arrive at an identifiers --*).

24. **With respect to claim 17**, Buchanan discloses the system of claim 16, wherein the data source indicators are generated from information retrieved from the data sources (*page 2, ¶18– retrieve and output an identifier associated with the cell from the database, where maintains a plurality of cell characteristics –; page 5, ¶50, -- retrieved comparable data from compilers and other source. More particularly, when recording characteristics from library-derived cells may receive file or reports generated from remote library design entities. The file may contain compatible identifiers--; and page 5, ¶51, -- retrieve identifiers and related data from other database containing library source--*).

25. **With respect to claim 18**, Buchanan discloses the system of claim 16, wherein a plurality of the bit vectors are processed by the processor to generate formatted

output (*figure 1 and 2, page 3, ¶18, -- output an identifiers associated with the cell from database--; page 5,* ¶51, -- *generating a library report as well as the extraction of identifying information and characteristics and related data from other database containing library resources -- page 5, ¶50, -- reports generated form remote library design entities --; and page 6,* ¶70, *the library reports may document cell characteristic that program code may process to arrive at an identifiers --*).

Response to Arguments

26. Applicant's arguments filed 03/20/2006 have been fully considered but they are not persuasive. Therefore, the claim rejection is maintained.

In the remarks, Applicant indicated that all limitations of every single claims can not anticipated by Buchanan.

Examiner respectfully does not agreed with Applicant arguments. Examiner points out more detail of every single limitation recited in each claim as claim rejection above to address all applicant arguments recited in remarks filed on 03/20/2006, pages 9-16. Applicants are advised to review the claim rejection.

Conclusion

27. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nghia M. Doan whose telephone number is 571-272-5973. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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05/01/2006